Laboratory 3

(Due date: **002/003**: February 17th, **004**: February 18th, **006**: February 19th)

OBJECTIVES

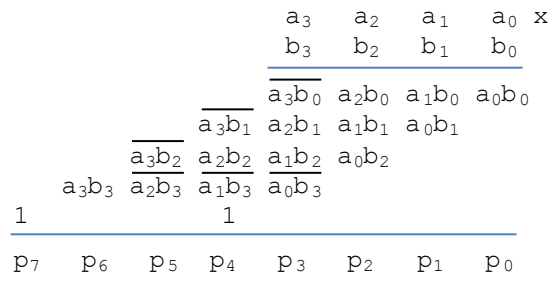
- ✓ Use the Structural Description on VHDL.
- ✓ Test arithmetic circuits on an FPGA.

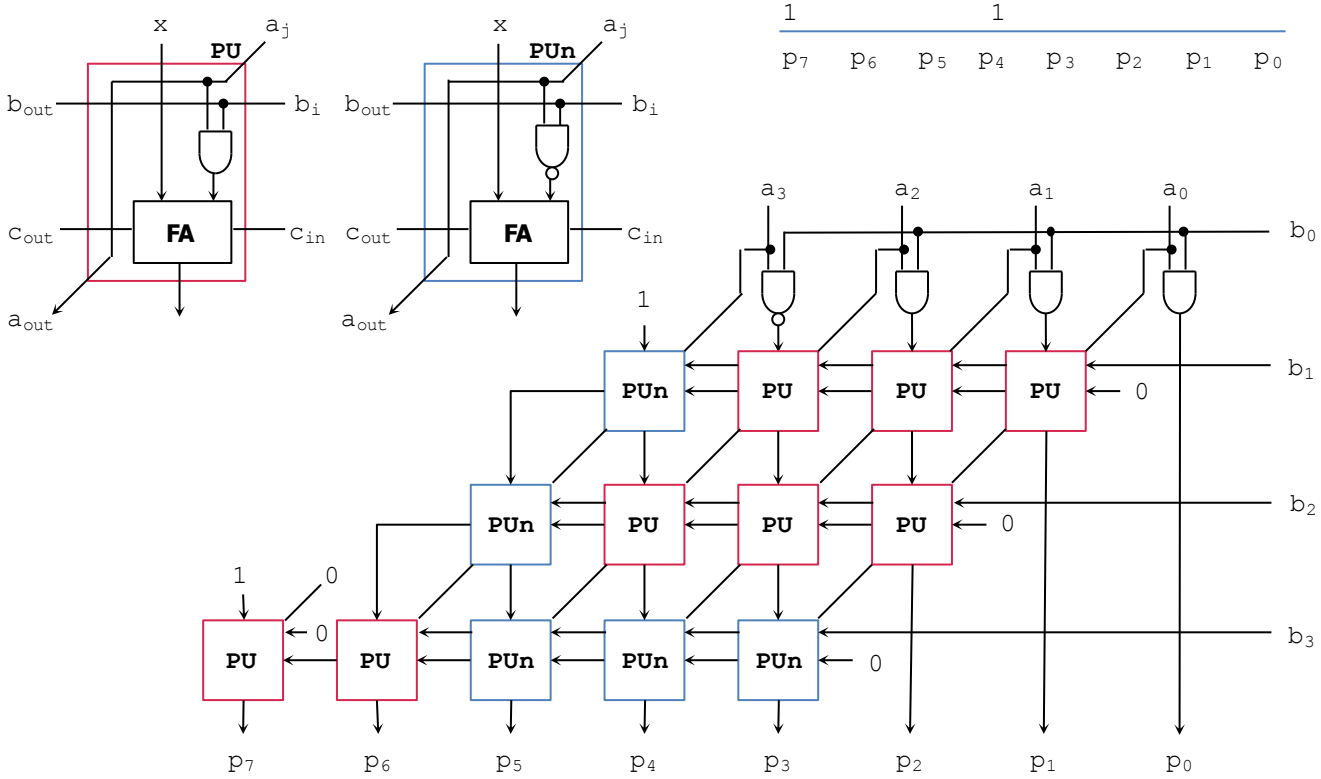
VHDL CODING

- ✓ Refer to the Tutorial: VHDL for FPGAs for a list of examples.

FIRST ACTIVITY (100/100)

- **PROBLEM**: The figure depicts a 2's complement array multiplier for two 4-bit signed numbers. It is based on the basic unsigned multiplier with some adjustments.





- ✓ **NEXYS A7-50T**: Create a new Vivado Project. Select the **XC7A50T-1CSG324 Artix-7 FPGA** device.
- ✓ Write the VHDL code for this signed array multiplier. Use the Structural Description: Create a separate file for the Full Adder, the Processing Unit (PU), the flipped Processing Unit (PUn) and the top file (Array Multiplier). Synthesize the code.
- ✓ Write the VHDL testbench to test the circuit for all possible cases (256 cases). Use 'for loop'.
- ✓ Perform Behavioral Simulation and Timing Simulation of your design. Make sure to represent data as signed (2C) integers (use Radix → Signed Decimal). **Demonstrate this to your TA**.
- ✓ I/O Assignment: Create the XDC file. Nexys-4: Use `SW0` to `SW7` for the inputs, and `LED7` to `LED0` for the output.
- ✓ Generate and download the bitstream on the FPGA and test. **Demonstrate this to your TA**.

- Submit (as a .zip file) the five generated files: VHDL code (4 files), VHDL testbench, and XDC file to Moodle (an assignment will be created). DO NOT submit the whole Vivado Project.

TA signature: _____ **Date:** _____

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